What is claimed is:

- 1 1. A designer configurable processor comprising:
- a. a plurality of designer configurable computational units operating in parallel;
- b. a memory device that communicates with the plurality of computational units through a
 data communication module; and
- 5 c. a software development tool that configures the plurality of computational units and a data path though the data communication module.
- 1 2. The processor of claim 1 wherein the designer configurable processor comprises a Very
 Long Instruction Word (VLIW) processor task engine.
 - 3. The processor of claim 1 wherein the data communication module comprises a register routed data communication module.
 - 4. The processor of claim 1 wherein the memory device stores at least one of data and instruction code.
 - 5. The processor of claim 1 further comprising a task queue that communicates with the data communication module, the task queue scheduling tasks for the processor.
 - 1 6. The processor of claim 5 wherein the task queue comprises a task queue controller module
 - 2 that communicates with the data communication module and a task queue module that
 - 3 communicates with task queue bus.

- 1 7. The processor of claim 6 further comprising an instruction memory that communicates with
- 2 the task queue controller module, the instruction memory storing tasks for the processor.
- 1 8. The processor of claim 1 wherein the software development tool comprise at least one of a
- 2 compiler, an assembler, an instruction set simulator, or a debugging environment.
- 9. The processor of claim 1 wherein the software development tool comprises a graphical
- 2 interface that visually illustrates the configuration of the processor.

2 RTL description of the processor.

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- 1 11. The processor of claim 1 wherein the software development tool configures a data path from
- 2 the processor to an input/output module.
- 1 12. The processor of claim 11 wherein the software development tool configures a width of the
- 2 data path from the processor to the input/output module.
- 1 13. The processor of claim 1 wherein the software development tool configures a data routing
- 2 path of at least one of the plurality of computational units.
- 1 14. The processor of claim 1 wherein the software development tool configures an instruction 1 2 1 1 execution speed of at least one of the plurality of computational units.
 - 15. The processor of claim 1 wherein the software development tool configures an energy required to operate at least one of the plurality of computational units.
 - 16. The processor of claim 1 wherein the software development tool configures an instruction set of at least one of the plurality of computational units.
 - 17. The multi-processor system of claim 1 wherein at least one of the plurality of designer configurable computational units comprises a set of input registers and a set of result registers.
 - 1 18. A designer configurable multi-processor system comprising:
 - 2 a. a plurality of designer configurable processors, each of the plurality of processors 3 comprising a plurality of designer configurable computational units operating in parallel;
 - 4 b. a memory device that communicates with the plurality of computational units through a 5 data communication module;
 - 6 c. an input/output (I/O) module that communicates with at least one of the plurality of 7 processors through an I/O bus; and
 - 8 d. a software development tool that configures the multi-processor system.

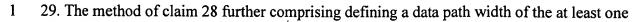
- 1 19. The multi-processor system of claim 18 wherein at least one of the plurality of plurality of
- 2 processors comprises a Very Long Instruction Word (VLIW) processor.
- 1 20. The multi-processor system of claim 18 further comprising an instruction memory device
- 2 that communicates with at least one of the plurality of processors.
- 1 21. The multi-processor system of claim 18 wherein the software development tool generates a
- 2 synthesizable RTL description of at least one of the plurality of processors.
- 1 22. The multi-processor system of claim 18 wherein the software development tool configures a
- 2 data path to the I/O module.
- 1 23. The multi-processor system of claim 22 wherein the software development tool configures a width of the data path to the I/O module.
 - 24. The multi-processor system of claim 18 wherein the software development tool configures a data routing path of at least one of the plurality of computational units.
 - 25. The multi-processor system of claim 18 wherein the software development tool configures an instruction execution speed of at least one of the plurality of computational units.
- 26. The multi-processor system of claim 18 wherein the software development tool configures an energy required to operate at least one of the plurality of computational units.
 - 1 27. The processor of claim 18 wherein the software development tool configures an instruction
 - 2 set of at least one of the plurality of computational units.
 - 1 28. A method of defining a computational unit for a multi-processor hardware system, the
 - 2 method comprising:

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- 3 a. defining an architecture of at least computation unit in a Very Long Instruction Word (VLIW) processor with a software development tool; and 4
- 5 b. generating data from the software development tool that integrates the at least one 6 computation unit into the VLIW processor task engine.



- 2 computation unit with the software development tool.
- 1 30. The method of claim 28 further comprising defining an internal data routing path of the at
- 2 least one computation unit with the software development tool.
- 1 31. The method of claim 28 further comprising defining an energy used to operate the at least
- 2 one computation unit with the software development tool.
- 1 32. The method of claim 28 further comprising defining an instruction speed of the at least one
- 2 computation unit with the software development tool.
- 33. The method of claim 28 further comprising defining an instruction set of the at least one
 computation unit with the software development tool.
 - 34. The method of claim 28 further comprising performing a consistency check to validate the multi-processor hardware system.
 - 35. The method of claim 28 wherein the generating data from the software development tool comprises generating scripts for an electronic design automation tool.